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Santanu Dutta

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EXAMINER

MALZAHN, DAVID H

ART UNIT

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2193

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**Technology Center 2100**

**BEFORE THE BOARD OF PATENT APPEALS  
AND INTERFERENCES**

Application Number: 10/005,551  
Filing Date: November 08, 2001  
Appellant(s): DUTTA ET AL.

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Robert J Crawford  
For Appellant

**EXAMINER'S ANSWER**

This is in response to the appeal brief filed 13 March 2006 appealing from the Office action  
mailed 17 October 2005.

**(1) Real Party in Interest**

A statement identifying by name the real party in interest is contained in the brief.

**(2) Related Appeals and Interferences**

The examiner is not aware of any related appeals, interferences, or judicial proceedings which will directly affect or be directly affected by or have a bearing on the Board's decision in the pending appeal.

**(3) Status of Claims**

The statement of the status of claims contained in the brief is correct.

**(4) Status of Amendments After Final**

The appellant's statement of the status of amendments after final rejection contained in the brief is correct.

**(5) Summary of Claimed Subject Matter**

The summary of claimed subject matter contained in the brief is correct.

**(6) Grounds of Rejection to be Reviewed on Appeal**

The appellant's statement of the grounds of rejection to be reviewed on appeal is correct.

**(7) Claims Appendix**

The copy of the appealed claims contained in the Appendix to the brief is correct.

**(8) Evidence Relied Upon**

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**(9) Grounds of Rejection**

The outstanding 35 U.S.C. 112(2) rejection of claims 1-19 is hereby withdrawn.

The following ground of rejection is applicable to the appealed claims:

Claims 1-19 stand rejected under 35 U.S.C. 102(b) as being anticipated by Daniels et al  
(Daniels).

Exemplary claim 1 may be read on Daniels (note the abstract) in the following manner:

Claim 1	Daniel's abstract
"a first binary operand of N bits"	the 16-bit operand
"a second binary operand of M bits"	the 8-bit operand
"an adder"	the 8-bit adder circuit
"sets of least-significant bits of the first and second binary operands"	the least significant byte of the 16 bit operand and the 8-bit operand
"a least-significant bits partial sum"	the least significant byte of the result
"a carryout"	as carry signal i.e. carry-out
"a multiplexer circuit"	the last sentence of the abstract describes the multiplexer circuit and it is shown in Figs. 1, 4A and 5-7
"a most-significant bits partial sum"	the most significant byte of the result
"set of most-significant bits of the first binary operand"	the most significant byte of the 16-bit operand which which is stored in the temporary register
"an offset of the representative set of most-significant bits of the first binary operand"	the output of the increment/decrement network which has inputted the most significant byte of the 16- bit operand and output offsets
"selection data being a function of the most-significant bit of the representative set of least-significant bits of the first binary operand"	the carry signal, i.e. carry-out, is a function the most significant bit of the least significant byte of the 16-bit operand

The other two independent claims, namely claims 18 and 19 may be read on Daniels in a similar manner.

#### **(10) Response to Argument**

Contrary to appellants' remarks Daniels clearly show a multiplexer circuit, note the last line of the abstract and Fig. 7, wherein either the output of the increment/decrement network (INCH) or the output of the temporary register (TEMPH) is feed to a single location (ABH).

Also contrary the appellants' remarks the selection data for the multiplexer is a function of the most-significant bit of the set of least-significant bits of the first binary operand because Daniels' carry-out is a function of the most significant bit of the least significant byte of the 16-bit operand and the carry-out is part of the selection data, note the last lines of the abstract and Fig. 5 which shows B7C being a function of carry-out and Fig. 7 which shows B7C is selection data for the multiplexer circuit. Also note that in the last full paragraph of page 6 of appellants' Appeal Brief appellants argue that since C15 is a selection bit and since C15 is a function of the MSB of the set of LSBs of the first binary operand then the selection data is a function of the MSB of the set of LSBs of the first binary operand.

Relative to claim 4, while Daniels does not explicitly call for N being 24 and M being 16 it is inherent in Daniel because Daniel speaks in terms of bytes, i.e. 8 bits, and his example is N being 16 and M being 8.

Relative to claim 16, Daniels does select one of at least three input binary quantities because Daniels increment/decrement network output an incremented quantity and decremented

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quantity and the temporary register outputs another quantity. Also note the many quantities are selectively fed to ABH.

Relative to claim 11, Daniels Fig. 4A illustrates the multiplexer circuit configured to operate as an exclusive-or gate, e.g. note elements 64, 67 and 69.

Relative to claim 15, Daniels system can operate on unsigned binary numbers.


Relative to claim 16 "a digital filtering circuit arrangement" is merely intended use.

#### **(11) Related Proceeding(s) Appendix**

No decision rendered by a court or the Board is identified by the examiner in the Related Appeals and Interferences section of this examiner's answer.

For the above reasons, it is believed that the rejections should be sustained.

Respectfully submitted,

  
David H. Malzahn

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